Flex Logix is a reconfigurable computing company providing leading edge eFPGA and AI Inference technologies for semiconductor and systems companies. Flex Logix eFPGA enables volume FPGA users to integrate the FPGA into their companion SoC, resulting in a 5-10x reduction in the cost and power of the FPGA and increasing compute density which is critical for communications, networking, data centers, microcontrollers and others. Its scalable AI inference is the most efficient, providing much higher inference throughput per square millimeter and per watt. Flex Logix supports process nodes from 180nm to 7nm; and can support other nodes on short notice. Flex Logix is headquartered in Mountain View, California and has an office in Austin, Texas. For more information, visit https://flex-logix.com.

Flex Logix looking for Physical Design Engineers (Senior Engineer/Principal) to join our growing team.

Responsibilities

- Generate block level static timing constraints and run STA
- Build IP floor-plan including pin placement, partitions and power grid.
- Develop and validate high performance low power clock network guidelines.
- Perform block level place and route and close the design to meet timing, area and power constraints.
- Generate and Implement ECOs to fix timing, noise and EM IR violations.
- Run Physical design verification flow at block level and provide guidelines to fix LVS/DRC violations to other designers.
- Participate in establishing CAD and physical design methodologies for correct construction designs.

Required Experience

- Bachelors or Master's Degree in EE/CS required.
- 7+ years of Physical Design experience on IP and/or SOC designs.
- Experience in developing and implementing Power-grid and Clock specifications.
- Deep knowledge about industry standards and practices in Physical Design, including Physically aware synthesis, floor-planning, and place & route.
- Deep understanding of scripting languages such as Perl/Tcl,
- Basic understanding of Extraction and STA methodology and tools.
- Deep understanding of Physical Design Verification methodology to debug LVS/DRC issues at block level.
- Strong understanding of all aspects of Physical construction, Integration and Physical Verification.
- Knowledge of Basic HDL languages like Verilog to be able to work with logic design teams for timing fixes.